In re Patent Application of:
PIO
Serial No. 09/779,956
Filed: FEBRUARY 9, 2001

Applicant again thanks the Examiner for the careful and thorough examination of the present application. Claims 8-25 remain pending in the application, with Claims 8-17 being directed to the elected invention. Favorable reconsideration of the rejection is respectfully requested.

Claims 8-17 were rejected in view of Patelmo et al. (EP No. 0996161) for the reasons set forth on page 2 of the Office Action. In view of the following remarks, favorable reconsideration of the rejection under 35 U.S.C. §102(e) is requested.

The present application is a divisional application of application Serial No. 09/364,766 filed July 30, 1999 and which claims foreign priority under 35 U.S.C. §119 of an Italian application (MI 98 001769) filed July 30, 1998, a certified copy of which is submitted concurrently herewith. The cited European patent publication (EP No. 0996161) was published on April 26, 2000 and filed on October 20, 1998. Accordingly, as acknowledged by the Examiner, the cited reference does not qualify as prior art against the present application.

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

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Lastly, Applicant requests the Examiner to acknowledge consideration of the Information Disclosure Statement filed March 14, 2001.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9318 to the MAIL STOP NON-FEE AMENDMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 this 3rd day of February, 2004.

STATEMENT OF TRANSLATOR

I, Barbara Ferrari, of Botti & Ferrari S.r.l., Via Locatelli, 5, I-20124 Milano, Italy, do hereby declare that I am conversant with English and Italian languages and that the following, to the best of my knowledge, is a true and accurate translation of the certified copy of the Italian Patent Application No. MI98A001769 filed on July 30, 1998.

June 24, 2003
Date

Signature

Barbara Ferrari
Printed Name

STM015BIT\LP\98-AG-047
STMicroelectronics S.r.l.

DESCRIPTION

FIELD OF APPLICATION

The present invention concerns an electronic memory circuit.

More specifically, the invention concerns an electronic memory circuit comprising a matrix of EEPROM memory cells, each of which incorporates:

- a MOS floating gate transistor and
- a selection transistor,

the matrix of the type comprising a plurality of rows and columns, each row being provided with a word line and each column comprising a bit line organized in line groups so as to group said matrix cells in bytes, each of which has a control gate line associated .

PRIOR ART

As known, the EEPROM memory arrangements, while being of a non-volatile type, allow to modify electrically the information therein contained, in either write and erase step.

It is also known that each EEPROM cell comprises a floating gate transistor and a selection transistor. Once the selection transistor is enabled, it is possible to alter the state of the associated floating gate transistor, by exploiting a passage of electrons for tunnel effect through a thin layer of silicon oxide, the so-called tunnel oxide; such thin layer is provided below a portion of the floating gate region of the floating gate transistor, in which the electric charge is stored.

During the steps of write and erase of the cells, positive voltages are usually employed, applied to the diffusion below the tunnel region or to the control gate. Such voltages are comprised between 8 and 18 Volt in order to generate at the opposite ends of the thin oxide a sufficiently high electrical field to activate efficiently the tunnel effect.

According to the prior art, the matrix consists of a structure 1' comprising a plurality of rows 3' and a plurality of columns 4'. Rows 3' comprise the so-called Word Lines WL'1, ..., WL'm. Columns 4' comprise instead the so-called Bit Lines BL' of the matrix and the Control Gate Lines CG'.

Preferably, the Bit Lines BL' are grouped in bytes 9', that is to say in groups of eight bits, BL'0 ..... BL'7.

In particular, each byte 9' has a line CG' associated.

At the crossing of a word line WL' and of a bit line BL', a selection transistor 5' is provided. Further on, a bit line BL' connects together all the drain terminals of the selection transistors 5' common to a given column 4' of the matrix. Every selection transistor 5' is associated and connected in series to a MOS floating gate transistor 2a'.

More in detail, the EEPROM memory cell 2' comprises a MOS transistor 2a' with a first region of floating gate 6' wherein the electrical charge is stored that allows to distinguish the two different states of the cell: "written" or "erased".

A second, so-called control gate region 7', is capacitively coupled to the floating gate region 6' through an intermediate, so-called interpoly dielectric layer. Through such dielectric layer voltage is transferred to the floating gate region 6' from the control gate region 7', during the write and/or erase steps of the cell 2'.

The control terminal of the control gate region 7' is common to all the cells 2' forming a same byte 9' in the structure 1'.

The erase of a byte 9' is accomplished addressing the word line WL'i corresponding to the desired i-th line and the control gate line CG'j corresponding to the selected byte.

The process for realizing on a silicon substrate of P-type these memory cells with the control gate region self-aligned with the floating gate region, foresees according to the prior art:

the formation of active areas;

the implantation of doped regions of N+ type;

the formation of oxides of different thickness;

the deposition and the following selective removal of a first layer of polysilicon for defining the floating gate regions in the direction of the Word Lines;

the formation of an interpoly dielectric;

the deposition and the following selective removal of a second layer of polysilicon for defining the control gate lines and the floating gate regions self-aligned to the control gate regions;

the implantation of the source and drain regions.

In order to guarantee the good operation of the matrix it is required that the control gate line CGj of each byte be electrically separated from the control gate line of the other bytes.

During the formation of the floating gate regions, the first layer of polysilicon between the floating gate regions belonging to adjacent cells of the same byte is removed; this step defines the floating gate regions in the direction of the line.

In order to minimize the area of each cell, it is desirable that the control gate lines of adjacent bytes be very close to each other. Therefore, during the above-described process step, the first layer of polysilicon is removed also by the source line portion common to two adjacent bytes.

As previously described, after the above step is carried out, an intermediate oxide layer and then the second layer of polysilicon are formed, in order to realize the region of control gate. In order to realize the final gate region of the floating gate transistor, a selective removal of the stack consisting of the second layer of polysilicon, of the dielectric interpoly layer and of the first layer of polysilicon, respectively is carried out.

This last removal is required in the process for realizing the final gate region and defines the length thereof.

In the portion of the source region common to two bytes, wherein the first layer of polysilicon had been removed during the first step of definition of the floating gates, the second step of removal of the first layer of polysilicon for defining the final gate region, is not selective enough for discriminating the first layer of polysilicon or the surface of the substrate of silicon in single-crystal form.

Therefore, the surface of the source region has notches 30 as shown in figure 5.

This surface arrangement of the common source region has various drawbacks. First of all these notches may become receptacles for contaminating material, hard to be removed because of the small dimensions of the notches 30 themselves.

Further on, because of the differences in height present on the surface of the source region, the subsequent implantation of dopant provides a not uniform implanted region. This situation increases the resistance of the common source region.

This drawback is particularly significant for the EEPROM parallel access memory matrixes, in that all the cells of the same byte will be read at the same time and hence the current in the common source region will reach relatively high values, that, because of the resistance introduced by the presence of these notches, may lead to a read error on the single memory cell.

SUMMARY OF THE INVENTION

The resolutive idea at the basis of the present invention is that of realizing an electronic memory circuit wherein the control gate line is electrically common to pairs of cells belonging to the same byte.

On the basis of such resolutive idea, the technical problem is solved by an electronic memory circuit comprising a matrix of EEPROM memory cells, each incorporating:

- a MOS floating gate transistor and
- a selection transistor,

the matrix of the type comprising a plurality of rows and columns, each row being provided with a word line and each column comprising a bit line organized in line groups so as to group said matrix cells in bytes, each of which has a control gate line associated, characterized in that

a pair of cells having a common source region, each cell being arranged symmetrically with respect to said common source region, has a common control gate region.

Advantageously, the common control gate region covers the common source region.

Features and advantages of the electronic memory circuit according to the present invention will result from the hereafter description out of an indicative but not restrictive embodiment with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In such drawings:

Fig. 1 shows a schematic view of a circuit structure realized according to the prior art;

Fig. 2 shows in enlarged scale a schematic view from above of a portion of semiconductor wherein an EEPROM memory cell is realized included in the circuit structure according to the prior art;

Fig. 3 shows in enlarged scale a schematic view in vertical section, taken along the line III-III of fig. 2 of a portion of semiconductor, wherein an EEPROM memory cell according to the prior art is realized;

Fig. 4 shows in enlarged scale a schematic view in vertical section, taken along the line IV-IV of fig. 2 of a portion of semiconductor, wherein an EEPROM memory cell according to the prior art is realized;

Fig. 5 shows in enlarged scale a schematic view in vertical section, taken along the line V-V of fig. 2 of a portion of semiconductor, wherein an EEPROM memory cell according to the prior art is realized;

Fig. 6 shows a schematic view of an electronic circuit realized according to the invention;

Fig. 7 shows in enlarged scale a schematic view from above of a portion of semiconductor wherein an EEPROM memory cell is realized included in the electronic circuit according to the invention;

Fig. 8 shows in enlarged scale a schematic view in vertical section, taken along the line VIII-VIII of fig. 7 of a portion of semiconductor, wherein EEPROM cells according to the invention are realized;

Fig. 9 to 17 show the process steps for realizing the EEPROM memory cells according to the invention;

Fig. 17 shows in enlarged scale a schematic view in vertical section, taken along the line XVII-XVII of fig. 7;

Fig. 18 shows in enlarged scale a schematic view in vertical section, taken along the line XVIII-XVIII of fig. 7;

Fig. 19 shows a second embodiment of the circuit according to the invention;

Fig. 20 shows a third embodiment of the circuit according to the invention.

DETAILED DESCRIPTION

With reference to such drawings, an electronic memory circuit consisting of a matrix of EEPROM memory cells 2 is wholly and schematically indicated with 1.

The structure 1 is realized as semiconductor integrated circuit, incorporating thousands of cells 2. In fig. 6 only a portion of such circuit is indicated, though.

The matrix according to the invention consists of a plurality of rows 3, comprising the so-called word lines WL1, WLm and a plurality of columns 4 comprising the so-called bit lines of the matrix.

The columns 4 comprise also the so-called control gate lines CG.

Groups of eight lines of bit, BL0, BL1 ... BL7 are grouped in a byte 9a.

For each byte 9a a memory cell 2 is connected to each bit line BLi.

Each EEPROM cell 2 comprises in a per se known way, a MOS transistor 2a in series to a selection transistor 5.

In particular each selection transistor comprises a source region 6a and a drain region 7 of N-type formed in a substrate 20 of P-type.

In a per se known way such region 7 comprises also a contact region 7a realized with an implantation of N+ type dopant.

A gate region 5a, insulated from the substrate 20, by means of the oxide layer 13 is comprised between the source region 6a and the drain region 7.

The gate region 5a comprises in a per se known way two superimposed regions of polysilicon 5b, 5c realized respectively in a first and second layer of polysilicon 14, 17 by means of the interposition of the intermediate dielectric layer 16; the two regions 5b, 5c are then electrically short-circuited outside the cell.

The floating gate transistor 2a comprises a region of source 6 and a region of drain 8, coincident with the source region 6a of the selection transistor 5.

In each floating gate transistor 2a, between the source region 6 and the drain region 8, the so-called channel region is provided, onto which a floating gate

region 11 is arranged, formed by the first layer of polysilicon 14 and insulated from the substrate by a layer of gate oxide 13 that has a thinner portion named tunnel oxide 10.

The drain region 8 is realized in the substrate by means of an implantation of N-type. In correspondence of this drain region 8, an implanted region 9 of N+ type is realized, that extends till below the tunnel region 10.

The source region 6 of the cell 1 is realized by means of an implantation of dopant of N-type in the substrate 2.

Advantageously, such region is common to pairs of cells 2 belonging to the same byte 9a.

Advantageously, the source region 6 and the implanted regions of type 9 may be realized with a same implantation of dopant of N+ type.

The source regions 6 of all cells 2 belonging to the same byte 9a form an only line of source.

The source lines are then connected to a common metallization line S.

Advantageously, the source lines of each byte column 9a are in contact with a respective source line Si (figure 19).

A so-called control gate region 12 is coupled capacitively to the floating gate region 11 by means of an intermediate layer of dielectric material, the so-called interpoly and is realized with the second layer 17 of polysilicon.

According to the invention, for each pair of cells, the control gate region 12 is physically and electrically connected and covers completely the common source region 6.

The control gate line CG is connected by means of an enabling transistor T to the control gate regions 12 of the pairs of cells.

This enabling switch T is realized by means of a per se known MOS transistor.

As shown in figure 6, pairs of cells belonging to the same byte 9a are addressed by two adjacent word lines WLm, WLm+1.

Another embodiment of the invention is shown in figure 20, wherein each byte 9b comprises four lines of bits BL0/4 , BL1/5, BL2/6, BL3/7.

For each byte 9, each bit line BLi is connected to two cells having in common the source region, such cells, as well, being addressed by two adjacent word lines WLm, WLm+1.

Advantageously, such an embodiment is even more compact.

More in particular, the process steps that lead to the realization of a matrix of cells according to the invention are described hereinbelow. The cells 2 of the matrix 1 are realized with MOS technology from a P-doped, semiconductor substrate 20.

The process for realizing the circuit according to the invention foresees in a known way:

the formation of active areas;

the implantation of N+ and/or N doped regions 6, 9;

the formation of oxides 10, 13 of different thickness.

According to the invention, a first layer 14 of polysilicon is deposited as shown in figure 9, that is selectively removed by means of a photolithographic process that foresees the use of a mask 15 for the source region 6.

The intermediate oxide layer 16 is then formed on the entire surface of the substrate 20 as shown in figure 10.

A second layer 17 of polysilicon is deposited (Fig. 11) and then selectively removed in order to form the control gate 12 of the pairs of cells 2 that have the source region 6 in common and the gate region of the selection transistor.

In this process step, there are also defined the floating gate regions 11 of the floating gate transistors 2a.

The process is complete with the following conventional steps that allow to attain:

- the implantation of the N-doped source and drain regions 7, 8 (Fig. 13);
- so called spacers 18 (Fig. 14);
- the N-channel and P-channel transistors of the circuitry associated to the structure 1;
- intermediate dielectrics.

A respective first and a second contact 19, 21 are then opened, covered by a first layer 20 and a second layer 22 of metallization, respectively, thereby forming the bit lines BL.

In figures 17 and 18 a detailed illustration is made of the realization of these contacts in the drain region of the selection transistor and of the bit lines BL. Nothing prevents, however, from forming such bit lines with the first metallic layer.

As shown in figure 6, the structure is of particularly reduced dimensions.

It is worth noting that in the prior art (Fig. 1), an enabling transistor T' of the Control Gate line CG' is provided for each word line WL'i.

In virtue of the symmetry of the matrix both in X- and Y-direction, in the semiconductor portion A of figure 1 four enabling transistors T' are provided.

Conversely, in the embodiment according to the invention, only one enabling transistor every two WL lines is required.

The circuit according to the invention may be therefore rendered compact, occupying a smaller area than the area of a conventional cell, in particular along the X direction, should the same technology be used.

The circuit according to the invention, realized according to the above described process resolves the technical problem and achieves several advantages, which are hereinbelow highlighted:

The provision of only one control gate region allows to avoid holes on the substrate surface wherein the source region of the EEPROM memory cells is realized.

Furthermore, the structural architecture of the memory cell according to the invention allows to save a step in the decoding process of the memory.

It now goes without saying that modifications and variations may be carried out on the herein described and illustrated memory cells, all falling within the scope of the invention, as defined in the following claims.

CLAIMS

1. Electronic memory circuit comprising a matrix of EEPROM memory cells, each incorporating:

- a MOS floating gate transistor (2a) and
- a selection transistor (5),

the matrix of the type comprising a plurality of rows (3) and columns (4), each row (3) being provided with a word line (WL) and each column (4) comprising a bit line (BL) organized in line groups so as to group said matrix cells in bytes (9a), each of which has a control gate line (CG) associated, characterized in that

a pair of cells (2) having a common source region (6), each cell (2) being arranged symmetrically with respect to said common source region (6), has a common control gate region (12).

2. Electronic circuit according to claim 1, characterized in that the pairs of cells (2), having the source region (6) in common, belong to the same byte (9a).

3. Electronic circuit according to claim 2, characterized in that the common control gate regions (12) of the pairs of cells belonging to the same byte are connected to the same control gate line (CG).

4. Electronic circuit according to claim 3, characterized in that an enabling transistor (T) addresses the common control gate line.

5. Electronic circuit according to claim 4, characterized in that said enabling transistor (T) is a MOS transistor.

6. Electronic circuit according to claim 1, characterized in that the common control gate region (12) covers the common source region (6).

7. Process for manufacturing an electronic memory circuit, comprising a matrix of EEPROM memory cells, comprising the steps of:

- formation of active areas;

- implantation of strongly doped regions (9);
- formation of layers (10, 13) of oxide of different thickness;
- implantation of a common source region (6);
- selective deposition of a first layer (14) of polysilicon;
- selective removal of said first layer from the common source region (6);
- deposition of an intermediate dielectric layer;
- deposition of a second layer (17) of polysilicon;
- realization of only one control gate region (12) for pairs of cells having the source region (6) in common.

TITLE

"ELECTRONIC MEMORY CIRCUIT AND RELATED MANUFACTURING METHOD"

ABSTRACT

An electronic memory circuit comprising a matrix of EEPROM memory cells, each of which incorporates:

- a MOS floating gate transistor (2a) and
- a selection transistor (5),

the matrix of the type comprising a plurality of rows (3) and columns (4), each row (3) being provided with a word line (WL) and each column (4) comprising a bit line (BL) organized in line groups so as to group said matrix cells in bytes (9A), each of which has a control gate line (CG) associated.

A pair of cells (2) having a common source region (6), each cell (2) provided symmetrically with respect to this common source region (6) has a common control gate region (12).